IN THE SPECIFICATION

Please r place paragraph [0024] with the following amended paragraph:

[0024] Figure 3 depicts an FPGA configuration 300 in which CLB R17C24, CLB R32C24, global clock buffer BUFG, and the identical circuit 205 of Figure 2**[[**A**]]** are interconnected to form a second ring oscillator. CLB R17C24, circuit 205, clock buffer BUFG, and the dashed portion of clock distribution network 110 and interconnect resources 215 and 220 are identical to the like-identified structures of Figure 2; consequently, the sum of the combined delay contributions of those dashed elements, "K" in equation 1, is identical in oscillator configurations 200 and 300. The portions of the oscillators depicted as connected via solid lines in the figures can be considered delay elements for which the difference in signal propagation delays provides a measure of clock skew. Including the delay elements in ring oscillators allows for accurate measures of propagation delay through the delay elements.

A1

Please replace paragraph [0038] with the following amended paragraph:

[0038] Skew measurements between vertical clock spines 110V may also be of interest, and can be combined with the above-described skew measurements to give a comprehensive skew analysis for an entire device. Patent Application Serial No. **[[**_____**]]**10/021,448 entitled "METHODS AND CIRCUITS FOR MEASURING CLOCK SKEW ON PROGRAMMABLE LOGIC DEVICES," by Siuki Chan, filed herewith ~~[docket number X-884]~~, describes methods of measuring skew between vertical clock spines and is incorporated herein by reference.

A2